DUTY CYCLE CORRECTION CIRCUIT OF DELAY LOCKED LOOP AND DELAY LOCKED LOOP HAVING THE DUTY CYCLE CORRECTION CIRCUIT

CROSS REFERENCES TO RELATED APPLICATIONS

[0001] This application claims priority under 35 U.S.C. § 119 from Korean Patent Application No. 2003-15863, filed on 13 March 2003, the entirety of which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND AND SUMMARY

[0002] Technical Field.

[0003] The present invention relates to a duty cycle correction circuit of a delay locked loop (DLL) and a delay locked loop including the duty cycle correction circuit, and more particularly to a duty cycle correction circuit including a switching circuit and a delay locked loop (DLL) including the duty cycle correction circuit, for efficiently analyzing the cause of generation of a duty cycle error.

[0004] Description.

[0005] Generally, a Delay Locked Loop (DLL) receives an external clock signal input from the outside of a system and generates an internal clock signal synchronized to the external clock signal. The system includes logic devices, semiconductor devices, etc., using the internal clock signal.

[0006] The DLL can be utilized in a cache memory device (instead of an SRAM device that is generally used) for increasing a data processing rate between a CPU and DRAM, or applied to a synchronous DRAM, a RAMBUS DRAM®, etc., as well as

various types of logic devices.

[0007] The Double Data rate (DDR) technique has been developed for improving the bandwidth of a memory system. A DDR memory system uses the rising edge and falling edge of the internal clock signal. The duty cycle of the internal clock signal is an important factor for maintaining the maximum timing margin in a high performance memory system.

[0008] When the duty cycle of the internal clock signal is not maintained at exactly 50%, the deviation of the duty cycle from 50% reduces the timing margin of a high performance memory system. For this reason, an apparatus for compensating for distortion of the duty cycle due to changes of processes, voltages, and temperatures, is necessary. A duty cycle correction circuit utilized in a DLL is a circuit for correcting the duty cycle of the internal clock signal.

[0009] FIG. 1 is a block diagram of a conventional delay locked loop (DLL). Referring to FIG. 1, the DLL 100 includes a DLL core 110, a clock buffer 130, and a duty cycle correction circuit 150.

[00010] The DLL core 110, an essential part of the DLL, receives an external clock signal ECLK and generates an internal clock signal ICLK synchronized to the external clock signal ECLK.

[00011] The clock buffer 130 includes a plurality of serially interconnected inverters 131, 133, 135, ... , 137, and buffers the internal clock signal ICLK to generate a reference clock signal CLK and a complementary reference clock signal CLKB.

[00012] The inverter 131 includes one PMOS transistor P1 and one NMOS transistor N1, which are serially connected between a source voltage VDD and a ground voltage VSS. The structures of the remaining inverters 133, 135, ... , 137 are the same as that of the inverter 131. The process for generating the reference

clock signal CLK and the complementary reference clock signal CLKB is well known in the art.

[00013] When the channel length to channel width ratio of the PMOS transistor P1 and NMOS transistor N1 is the same in each of the inverters 131, 133, 135, ... , 137, then the clock buffer 130 can output differential reference clock signals CLK and CLKB having a duty cycle of 50%.

[00014] However, if the duty cycle of the differential reference clock signals CLK and CLKB becomes 45% or 55% (hereinafter, referred to as "case when a duty cycle error is generated"), or not exactly 50%, due to changes in a process, voltage, and temperature, then the timing margin of the high performance memory system is reduced.

[00015] To avoid this problem, the duty cycle correction circuit 150 converts the differential reference clock signals CLK and CLKB into duty cycle offset information DCC and DCCB, and feeds back the duty cycle offset information DCC and DCCB to the DLL core 110. Thus, the DLL core 110 controls the duty cycle of the internal clock signal ICLK to be exactly 50% in response to the duty cycle offset information DCC and DCCB.

[00016] Since the duty cycle correction circuit 150 always operates while the DLL 100 is operating, it is not known whether the differential reference clock signals CLK and CLKB having the 50% duty cycle are generated by the interaction of the clock buffer 130 and the duty cycle correction circuit 150, or by the greater operation of the clock buffer 130 rather than that of the duty cycle correction circuit 150.

[00017] Thus, when a duty cycle error is generated, it is impossible to correctly analyze whether the duty cycle error is generated by the clock buffer 130 or by the duty cycle correction circuit 150.

[00018] Therefore, it would be desirable to provide a duty cycle correction circuit and a delay locked loop (DLL) including the duty cycle correction circuit, where the DLL is capable of controlling its operation in order to correctly analyze the cause of a duty cycle error when a duty cycle error is generated in the DLL.

[00019] According to one aspect of the present invention, a duty cycle correction circuit of a delay locked loop comprises: a differential amplifier which receives and amplifies differential reference signals input from a first input terminal and a second input terminal, and outputs differential output signals to a first differential output terminal and a second differential output terminal; a first transmission circuit which is connected between the first differential output terminal and a first node, and transmits a signal of the first differential output terminal to the first node under the control of control signals; a second transmission circuit which is connected between the second differential output terminal and a second node, and transmits a signal of the second differential output terminal to the second node under the control of the control signals; a first storage unit which is connected between the first node and a ground voltage and stores a signal of the first node; a second storage unit which is connected between the second node and the ground voltage and stores a signal of the second node; and a switching circuit which connects the first node to a first output terminal and the second node to a second output terminal under the control of a switching control signal.

[00020] The switching circuit comprises: a third transmission circuit which transmits the signal of the first node to the first output terminal when a switching control signal has a deactivated state; a fourth transmission circuit which transmits the signal of the second node to the second output terminal when the switching control signal has the deactivated state; a first voltage supplying circuit which is

connected between the first output terminal and the ground voltage, and supplies the ground voltage to the first output terminal when a switching control signal has an activated state; and a second voltage supplying circuit which is connected between the second output terminal and the ground voltage, and supplies the ground voltage to the second output terminal when the switching control signal has the activated state.

[00021] The first transmission circuit through the fourth transmission circuit each include a PMOS transistor and a NMOS transistor. The first storage unit and the second storage unit each include a MOS transistor.

[00022] According to another aspect of the present invention, a delay locked loop comprises: a DLL core which receives an external clock signal and generates an internal clock signal synchronized to the external clock signal; a buffer which buffers the internal clock signal and outputs differential reference clock signals; and a duty cycle correction circuit which generates first control signals having desired offsets corresponding to differences in the duty cycles of each of the differential reference clock signals, and outputs the first control signals to the DLL core under the control of a switching control signal, wherein the DLL core corrects a duty cycle of the internal clock signal under the control of the first control signals.

[00023] The delay locked loop further comprises a pad for receiving the switching control signal. The delay locked loop further comprises a mode register set for generating the switching control signal.

[00024] According to another yet aspect of the present invention, a duty cycle correction circuit, comprises: input terminal adapted to receive a pair of differential reference clock signals each having a duty cycle; integrating means for integrating each of the reference clock signals to produce a pair of control signals indicating the

duty cycles of the differential reference clock signals; and switching means adapted to receive a switching control signal and in response thereto to selectively output the control signals when the switching control signal has a first state and to output a pair of fixed voltage signals when the switching control signal has a second state.

BRIEF DESCRIPTION OF THE DRAWINGS

[00025] The above and other features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

[00026] FIG. 1 is a block diagram of a conventional delay locked loop;

[00027] FIG. 2 is a block diagram of a delay locked loop according to a preferred embodiment;

[00028] FIG. 3 is a circuit diagram of a duty cycle correction circuit of a delay locked loop, according to a preferred embodiment; and

[00029] FIG. 4 is an operation timing chart of the duty cycle correction circuit of the delay locked loop.

DETAILED DESCRIPTION

[00030] Hereinafter, embodiments of the present invention will be described in detail with reference to the appended drawings. In respective drawings, components denoted by a same reference number represent a same component.

[00031] FIG. 2 is a block diagram of a delay locked loop according to a preferred embodiment. Referring to FIG. 2, the delay locked loop (also, referred to as DLL) 200 includes a DLL core 210, a clock buffer 130, a duty cycle correction circuit 230, and a pad 240.

[00032] The DLL core 210 receives an external clock signal ECLK and generates an internal clock signal ICLK synchronized to the external clock signal ECLK. The clock buffer 130 buffers the internal clock signal ICLK and generates differential reference clock signals CLK and CLKB.

[00033] The duty cycle correction circuit 230 generates first control signals DCC and DCCB having desired offsets corresponding to differences between respective duty cycles of the differential reference clock signals CLK and CLKB, and outputs the first control signals DCC and DCCB to the DLL core 210. The generation and subsequent output of the control signals DCC and DCCB is performed under the control of a switching control signal DCC_CTL input from outside of the DLL 200 through the pad 240.

[00034] The DLL core 210 corrects the duty cycle of the internal clock signal ICLK under the control of the first control signals DCC and DCCB. The first control signals DCC and DCCB include duty cycle offset information.

[00035] The switching control signal DCC_CTL can be generated by a mode register set (MRS) or logic register.

[00036] FIG. 3 is a circuit diagram of the duty cycle correction circuit of the delay locked loop, according to a preferred embodiment. Referring to FIG. 3, the duty cycle correction circuit 230 includes a differential amplifier 231, a transmission circuit 233, a storage unit 235, and a switching circuit 237.

[00037] The differential amplifier 231 receives a reference clock signal CLK input via the gate (hereinafter, referred to as "a first input terminal") of an NMOS transistor N11 and a complementary reference clock signal CLKB input via the gate (hereinafter, referred to as "a second input terminal") of an NMOS transistor N13, amplifies the difference between both reference clock signals CLK and CLKB, and

outputs the amplified differential output signals to a first differential output node ND6 and a second differential output node ND7, respectively.

[00038] The transmission circuit 233 includes a first transmission circuit TG1 and a second transmission circuit TG2. The first transmission circuit TG1 is comprised of a PMOS transistor P29 and an NMOS transistor N47. The second transmission circuit TG2 is comprised of a PMOS transistor P33 and a NMOS transistor N51.

[00039] The first transmission circuit TG1 is connected between the first differential output terminal ND6 and a first node ND8, and transmits a signal of the first differential output terminal ND6 to the first node ND8 under the control of control signals CAP_ON and CAP_ONB.

[00040] The second transmission circuit TG2 is connected between the second differential output terminal ND7 and a second node ND9, and transmits a signal of the second differential output terminal ND7 to the second node ND9 under the control of the control signals CAP_ON and CAP_ONB. The control signals CAP-ON and CAP-ONB are complementary signals.

[00041] The storage unit 235 includes a first storage unit N55 and a second storage unit N57. The first storage unit N55 is connected between the first node ND8 and a ground voltage VSS and stores the signal of the first node ND8. The first storage unit N55 is comprised of an NMOS transistor.

[00042] The second storage unit N57 is connected between the second node ND9 and the ground voltage VSS and stores the signal of the second node ND9. The second storage unit N57 is also comprised of an NMOS transistor.

[00043] The switching circuit 237 connects the first node ND8 to a first output node ND10, and the second node ND9 to a second output node ND11, respectively, under the control of a switching control signal DCC_CTL. The switching circuit 237

includes a third transmission circuit TG3, a fourth transmission circuit TG4, a first voltage supplying circuit N67, and a second voltage supplying circuit N69.

[00044] The third transmission circuit TG3 is comprised of a PMOS transistor P37 and an NMOS transistor N59, and transmits the signal of the first node ND8 to the first output terminal ND10 when the switching control signal DCC_CTL is in a deactivated state (logic "low").

[00045] The fourth transmission circuit TG4 is comprised of a PMOS transistor P41 and a NMOS transistor N63, and transmits the signal of the second node ND9 to the second output terminal ND11 when the switching control signal DCC_CTL is in the deactivated state (logic "low").

[00046] The first voltage supplying circuit N67 is connected between the first output terminal ND10 and the ground voltage VSS, and supplies the ground voltage VSS to the first output terminal ND10 when the switching control signal DCC_CTL is activated (logic "high"). When the first voltage supplying circuit N67 is implemented by an NMOS transistor, then the first output terminal ND10 is pulled down to the ground voltage VSS when the switching control signal DCC_CTL is activated.

[00047] The second voltage supplying circuit N69 is connected between the second output terminal ND11 and the ground voltage VSS, and supplies the ground voltage VSS to the second output terminal ND11, when the switching control signal DCC_CTL is in the activated. When the second voltage supplying circuit N69 is implemented by a NMOS transistor, then the second output terminal ND11 is pulled down to the ground voltage VSS when the switching control signal DCC_CTL is activated.

[00048] The operation of the duty cycle correction circuit 230 of the delay locked loop will now be described with reference to FIGs. 2 and 3. First, the detailed

operation of the differential amplifier 231 is described as follows.

[00049] If a bias voltage VIAS output from the DLL core 211 is activated to a "high" level, NMOS transistors N15, N17, and N19 and PMOS transistors P11, P13, and P15, each of which acts as a current source, are turned-on, and accordingly the differential amplifier 231 is operated.

[00050] If a mode control signal NAPB is also activated to a "high" level, then the NMOS transistor N21 is turned-on, and the voltage of the node ND5 is pulled down to the ground voltage VSS via the turned-on NMOS transistors N21 and N19. Since the voltage of the node ND5 is pulled down to the ground voltage VSS, a PMOS type capacitor P17 and PMOS transistors P19, P21, and P23 each having a current mirror structure, are turned-on.

[00051] Also, the voltages of nodes ND1 and ND2 are differentially amplified by the NMOS transistors N11 and N13, respectively, which are turned-on or turned-off according to the states of the differential reference clock signals CLK and CLKB. The amplified signals of the nodes ND1 and ND2 are transferred to the first differential output terminal ND6 and second differential output terminal ND7 via the turned-on PMOS transistors P21 and P23, respectively.

[00052] Any output terminal being in a "high" level among the differential output terminals ND6 and ND7 is changed to a "low" level since a current path to the ground voltage VSS is formed through NMOS transistors N27, N29, N39, and N41 when they are turned on by the activation of the control signal CAP_ON.

[00053] Also, any output terminal being in a "low" level among the differential output terminals ND6 and ND7 is pulled up to a "high" level by a source voltage VDD supplied through the PMOS transistors P13, P15, P21, and P23 having a current mirror structure, since the current path to the ground voltage VSS is not formed.

[00054] Accordingly, when the bias voltage VIAS has a "high" level, the mode control signal NAPB has a "high" level, and a power reset signal PW_RESET has a "low" level, then a differential signal corresponding to the differential reference clock signals CLK and CLKB is output to the differential output terminals ND6 and ND7, respectively.

[00055] Meanwhile, in the case where the bias voltage VIAS has a "high" level, both the mode control signal NAPB and the control signal CAP_ON have "low" levels, and the power reset signal PW_RESET has a "high" level, the NMOS transistor N21 is turned-off, the PMOS transistor P25 is turned-on, and accordingly, the voltage of the node ND5 becomes a "high" level. Therefore, the PMOS type capacitor P17 and the PMOS transistors P11, P13, and P15 having the current mirror structure are turned-off, respectively.

[00056] When the respective NMOS transistors N27, N29, N39, and N41 are turned-off, the differential amplifier 231 does not operate. At this time, the differential output terminals ND6 and ND7 are equalized by the PMOS transistor P27.

[00057] The control signal CAP_ON is input into the gates of the NMOS transistors N47 and N51 and the gates of the PMOS transistors P31 and P35. The complementary control signal CAP_ONB is input into the gates of the NMOS transistors N49 and N53 and the gates of the PMOS transistors P29 and P33. The NMOS transistor N49 and PMOS transistor P31, and the NMOS transistor N53 and PMOS transistor P35 form capacitors.

[00058] The first transmission circuit TG1 transmits the signal of the first differential output terminal ND6 to the first node ND8 under the control of the control signals CAP_ON and CAP_ONB. The second transmission circuit TG2 transmits the signal of the second differential output terminal ND7 to the second node ND9 under the

control of the control signals CAP_ON and CAP_ONB.

[00059] The first storage unit N55 stores the signal (voltage) of the first node ND8 during a predetermined time period, and the second storage unit N57 stores the signal (voltage) of the second node ND9 during a predetermined time period.

[00060] The signal transmitted to the first node ND8 is transferred to the first output terminal ND10 when the switching control signal DCC_CTL has a "low" level, and also the signal transmitted to the second node ND9 is transferred to the second output terminal ND11 when the switching control signal DCC_CTL have the "low" level.

[00061] However, when the switching control signal DCC_CTL has a "high" level, then the third transmission circuit TG3 is turned-off, the fist output terminal ND10 is pulled down to the ground voltage VSS, the fourth transmission circuit TG4 is turned off, and the second output terminal ND11 is pulled down to the ground voltage VSS.

[00062] The switching control signal DCC_CTL is input into the gates of the respective PMOS transistors P37 and P41, the gates of the respective NMOS transistors N61, N65, N67, and N69, and an inverter I11. The output signal of the inverter I11 is input into the gates of the PMOS transistors P39 and P43 and the gates of the NMOS transistors N59 and N63. The NMOS transistor N61 and PMOS transistor P39, and the NMOS transistor N65 and PMOS transistor P43 form capacitors, respectively.

[00063] The duty cycle correction circuit 230 is turned on or turned off depending on the status of the switching control signal DCC_CTL.

[00064] FIG. 4 is an operation timing chart of the duty cycle correction circuit of the delay locked loop of FIGs. 2 and 3. The bias voltage VIAS, the mode control signal NAPB, and the control signal CAP_ON all have "high" levels ("H"), and the switching

control signal DCC_CTL has a "low" level ("L").

[00065] A case where the duty cycle of the reference clock signal CLK is 50% is described below with reference to FIGs. 2 through 4.

[00066] The differential amplifier 231 receives and amplifies the reference clock signal CLK input from the first input terminal and the complementary reference clock signal CLKB input from the second input terminal, and outputs the amplified result into the first differential output terminal ND6 and the second differential output terminal ND7, respectively.

[00067] The first storage unit N55 stores electric charge corresponding to the duty cycle (for example, 45%) of the complementary reference clock signal CLKB, and the second storage unit N57 stores electric charge corresponding to the duty cycle (for example, 55%) of the reference clock signal CLK.

[00068] Therefore, a predetermined DC offset is generated between a signal DCCB that is output to the DLL core 210 via the first output terminal ND10, and a signal DCC that is output to the DLL core 210 via the second output terminal ND11.

[00069] The DLL core 210 corrects the duty cycle of the internal clock signal ICLK in response to the signals DCC and DCCB output from the duty cycle correction circuit 230. Accordingly, due to repeated interaction between the duty cycle correction circuit 230 and the DLL core 210, the duty cycle of the reference clock signal CLK becomes 50%. If the duty cycle of the reference clock signal CLK is 50%, then the DC offset is zero. Otherwise, if the duty cycle of the reference clock signal CLK becomes more or less than 50%, then the DC offset increases.

[00070] However, if the switching control signal DCC_CTL is changed to a "high" level ("H"), then the signal of the first node ND8 is not transmitted to the first output terminal ND10, and also the signal of the second node ND9 is not transmitted to the

second output terminal ND11. Also, since the NMOS transistors N67 and N69 of the switching circuit 237 are turned-on when the switching control signal DCC_CTL has the high level, the output signal DCCB of the first output terminal ND10 and the output signal DCC of the second output terminal ND11 are pulled down to the ground voltage VSS. In this case, the electric charge stored in the first storage unit N55 and second storage unit N57 is maintained.

[00071] Accordingly, when the switching control signal DCC_CTL is changed to a high level ("H"), then the duty cycle of the reference clock signal CLK is determined depending on the inverters 131, 133, 135, ... , 137 constituting the clock buffer 130.

[00072] If the switching control signal DCC_CTL is changed into a low level ("L"), then the signal of the first node ND8 is transmitted to the first output terminal ND10 and the signal of the second node ND9 is transmitted to the second output terminal ND11, and the NMOS transistors N67 and N69 are turned-off.

[00073] Accordingly, the switching circuit 237 outputs to the DLL core 210 the signals DCC and DCCB just before the switching control signal DCC_CTL is changed to the high level ("H"). Thus, the DLL core 210 corrects the duty cycle of the internal clock signal ICLK in response to the signals DCC and DCCB output from the duty cycle correction circuit 230.

[00074] Therefore, when a duty cycle error is generated in the DLL 200 including the duty cycle correction circuit 230, the duty cycle of the reference clock signal CLK becomes exactly 50%, regardless of whether a duty cycle error is generated by the clock buffer 130, due to the duty cycle correction circuit 230, and/or due to the clock buffer 130 and duty cycle correction circuit 230.

[00075] As described above, according to the present invention, it is possible to correctly analyze the cause of generation of the duty cycle error when the duty cycle

error is generated in a DLL including the duty cycle correction circuit capable of being turned on or turned off. Therefore, in the DLL and the system including the DLL, debugging time can be minimized.

[00076] Also, it is possible to check whether the duty cycle correction circuit is operating correctly in a DLL including the duty cycle correction circuit according to the present invention.

[00077] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims.